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LARGE-SIGNAL MODELING OF GaAs POWER FET AMPLIFIERS

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ABSTRACT

A new large-signal, analytic model for the GaAs MESFET is used in conjunction with the modified harmonic balance technique to study the performance of a monolithic, C-band power FET amplifier. The new device model is physics based and requires device, material and bias data as input. The model includes the effects of non-uniform doping profiles and charge accumulation in the channel. Both small- and large-signal parameters calculated with the model are in good agreement with measured data. The power and harmonic performance of the complete amplifier are also in good agreement with measured data.

INTRODUCTION

In recent years significant progress has been made in the development of GaAs microwave monolithic integrated circuits. GaAs FETs are increasingly being used in large-signal microwave applications such as power amplifiers, oscillators, mixers and harmonic generators. The development of an accurate, nonlinear device model for the GaAs MESFET is essential to computer-aided design of microwave integrated circuits for large-signal applications. Small-signal GaAs FET amplifiers can be accurately designed with the aid of measured small-signal s-parameters. It is difficult to apply this methodology to the design of power amplifiers and other large-signal circuits in which nonlinear effects and multiple harmonics are simultaneously present in the circuit. There are three major empirical techniques presently used in the design of power FET amplifiers: (1) The load-pull method [1]; (2) 'large-signal' s-parameter measurements [2]; and (3) large-signal characterization by means of a bias dependent equivalent circuit extracted from small-signal s-parameter measurements [3]. These empirical methods, however, are very cumbersome and are more useful as analysis rather than systhesis tools. The empirical methods all require that the device be fabricated before it can be characterized. The need for accurate physical device models is more acute in GaAs MMIC design in which external tuning or tweaking of the circuit is difficult.

In this paper we present an application of a new, large-signal analytic model [4,5] which is used in combination with the method of modified harmonic balance to study the performance of a monolithic C-band power FET amplifier.

DEVICE MODEL

The new FET model incorporates two unique features: (1) It allows for arbitrary doping profiles, thereby permitting investigations of ion-implanted structures; and (2) It allows for charge accumulation in the channel in a self-consistent manner. It is shown that the accumulated charge can affect the output conductance and capacitances of the FET. Other features of the model include the presence of a smooth transition of charge between the channel and depletion region and the effect of velocity vector rotation on the output conductance. These effects have been shown to be significant factors in the operation of FETs, especially for operation in the saturation region [6].

The input parameters to the model consist of the doping profile data, device dimensions, material parameters, and parasitic resistances and reactances. Fig. 1 shows measured and modeled static I-V characteristics of a 1.0 μm gate length, ion-implanted power FET with a total grate width of 2.5 mm. The doping profile was modeled using LSS theory and the following parameters: dose = 4.5×10^{12} cm^{-2}, energy = 350 keV, cap thickness = 850 Å, and recess depth = 0.185 μm. The small-signal parameters of the FET were also calculated with the model and agree with those extracted from device s-parameter measuremnts. Fig. 2 shows the transconductance variation with gate-source voltage at a drain-source voltage of 3.0 v. A pinch-off voltage of -4.4 v was calculated and this is in good agreement with the measured value. Fig. 3 shows the gate-source capacitance as a function of gate-source voltage. As shown, Cgs decreases as Vgs approaches Vpo. Beyond pinch-off, the only contribution to Cgs comes from the fringing capacitance due to the charge distribution beyond the gate edges. Nonlinearities in gm and Cgs are the most important in large-signal operation of the device. Fig. 4 shows the variation in the gate-drain capacitance (Cgd) as a function of Vds at Vgs = 0. In the saturation region of operation where devices are generally biased, Cgd does not change significantly with Vds. The nonlinearity in output drain-source

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resistance (Rds) is also important to the overall transfer function. Fig. 5 shows Rds as a function of Vds. The drain-source resistance increases with Vds and with increasing gate-source voltage, as expected.

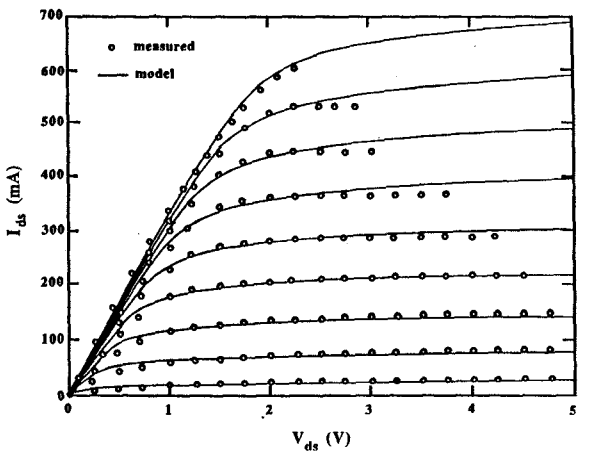

Fig. 1 Measures and Modeled Static I-V Characteristics for the 2.5 mm Device. Gate-Source voltages are 0, -0.5,..-4.5v.

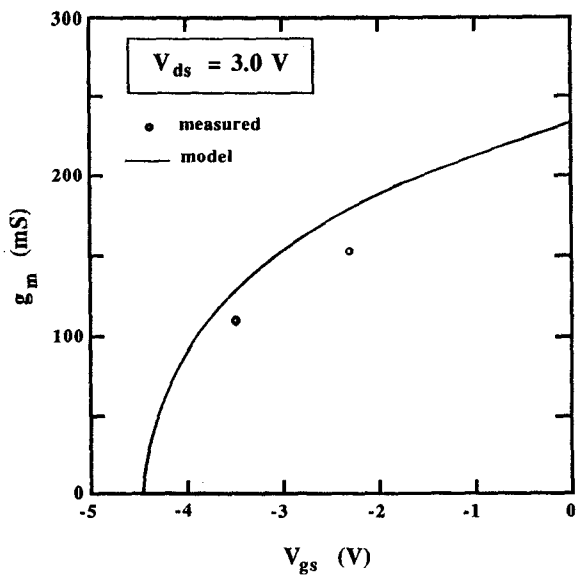

Fig. 2 Transconductance versus Vds at Vds = 3.0 v.

CIRCUIT SIMULATION

The power performance of the C-band monolithic circuit shown schematically in Fig. 6 was investigated with the FET model and the modified harmonic balance method. The amplifier circuit consists of two single-state amplifiers in parallel for a total output power of 3 W at 5.5 GHz. The FETs used in the amplifier have 4.0 mm total gate width each. The bias network for the gate and drain, as well as the input and output dc blocking capacitors were included in the RF simulaiton. Fig. 7 shows the output power at the fundamental versus the input power for the complete circuit. A small-signal gain of about 9 db was predicted which agrees well with the measured data. The calculated output power at the 1 db compression point is about 32 dbm. The power added efficiency of the amplifier is shown in Fig. 8 and has a maximum value of about 40% with an input power of 25 dbm.

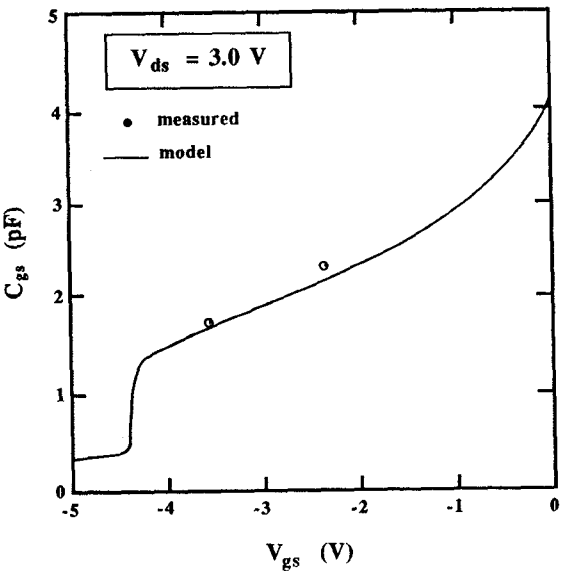

Fig. 3 Gate-Source Capacitance versus Gate-Source Voltage at Vds = 3.0 v.

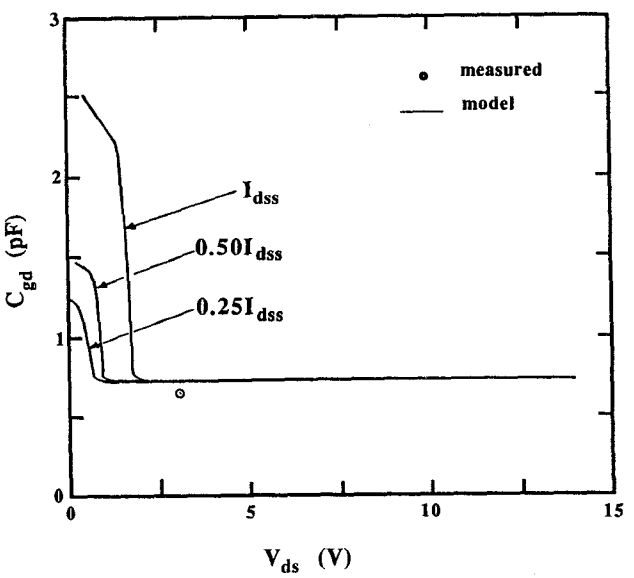

Fig. 4 Gate-Drain Capacitance versus Vds at Drain Currents of Idss, 1/2 Idss, and 1/4 Idss.

CONCLUSIONS

A new large-signal, analytic model for the GaAs MESFET is used to study the dc, small-signal and large-signal RF performance of a C-band monolithic power FET amplifier. Both small- and large-signal parameters are calculated and are shown to be in good agreement with experimental data. The new device model is useful in the analysis and optimization of monolithic FET circuits. It permits design studies of devices for given applications before fabrication.

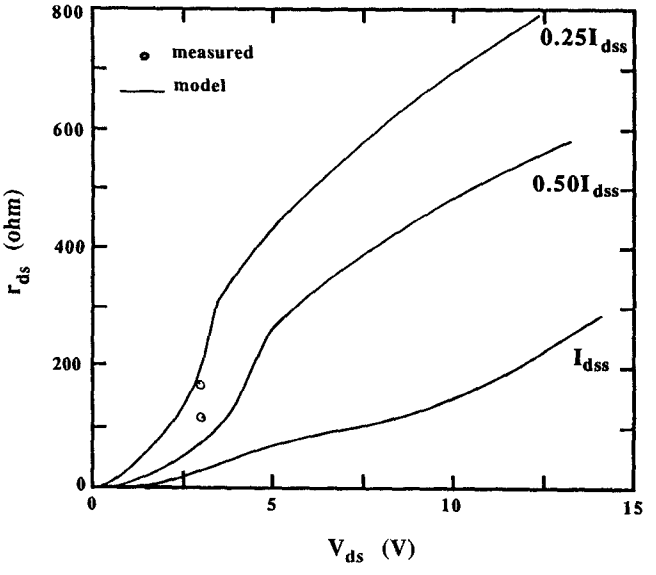

Fig. 5 Drain-Source Resistance as a Function of Vds at Drain Currents of Idss, 1/2 Idss, and 1/4 Idss.

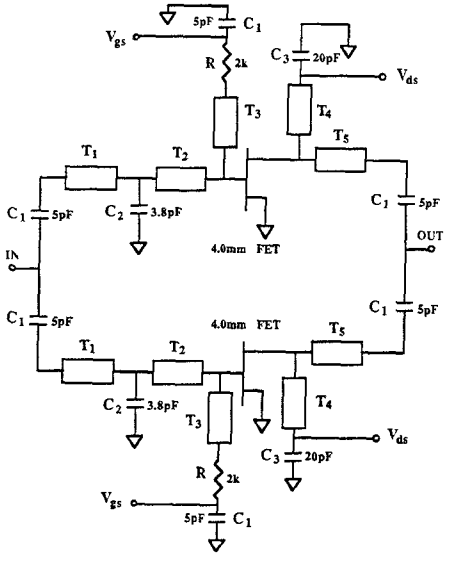

Fig. 6 Monolithic C-Band Power Amplifier Circuit.

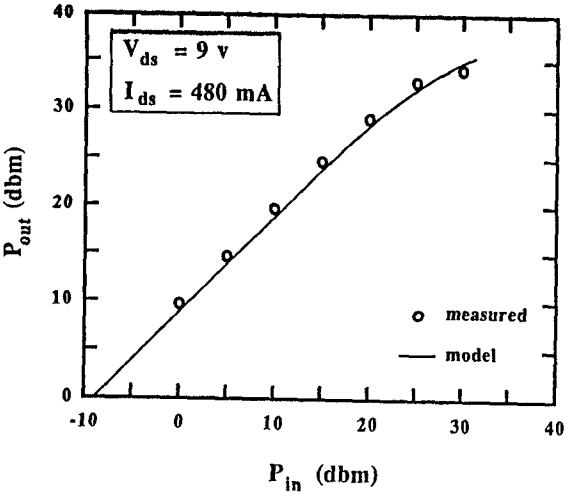

Fig. 7 Output Power at the Fundamental Frequency (5.5 GHz) versus Input Power for the Amplifier.

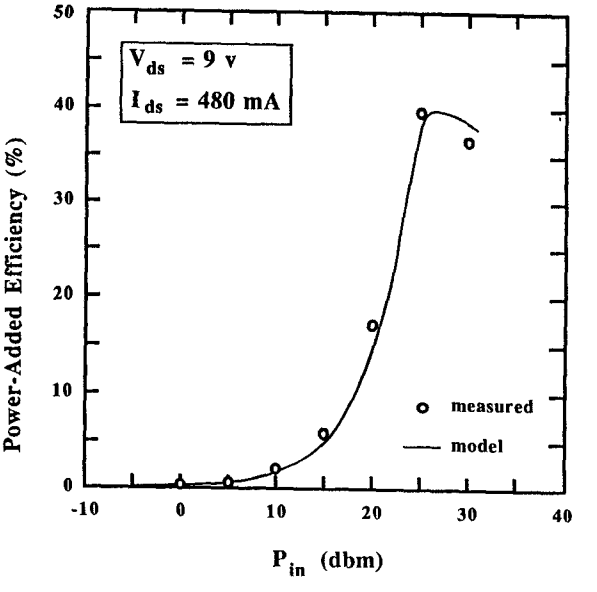

Fig. 8 Power-Added Efficeincy versus Input Power for the Amplifier.

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